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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/816,312	03/31/2004	Weimin Tchen	491442002000	9110

42178 7590 10/02/2007

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EXAMINER	
WANG, ALBERT C	

ART UNIT	PAPER NUMBER
2115	

MAIL DATE	DELIVERY MODE
10/02/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/816,312	TCHEN ET AL.	
	Examiner	Art Unit	
	Albert Wang	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 August 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 1 August 2007 has been entered.

Claim Rejections - 35 USC § 103

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 1-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chawla et al., U.S. Patent No. 6,442,067 (hereinafter "Chawla"), in view of Chen et al., U.S. Patent No. 2005/0125650 (hereinafter "Chen"), and Huang et al., U.S. Patent No. 7,162,568 (hereinafter "Huang").

As per claim 1, Chawla teaches in a processing unit including nonvolatile memory for storing executable code, the nonvolatile memory comprising a vital region for storing vital code and a region for storing less vital code (figs. 2 & 3, ROM 60; col. 6, lines 39-63, active image area and inactive image area), an apparatus for executing an update program for managing updates to the vital region of the nonvolatile memory with update code, the apparatus comprising:

a processor (col. 6, lines 23-34, processor 58) programmed for

performing a write test by writing test code into the less vital region to simulate an actual update to the vital region (col. 7, lines 17-25), and

performing an actual write of the update code into the vital region if the write test is successful (col. 7, lines 26-31).

Chawla does not express teach details of verifying test status and data of each block when writing code into multiple blocks in the nonvolatile memory. Chen teaches a processing unit including nonvolatile memory (par. 0046). Chen teaches confirming each segment when writing code into multiple segments into a nonvolatile memory (par. 0076). At the time of the invention, it would have been obvious to one of ordinary skill in the art that a piecemeal writing method similar to Chen's may be applied to Chawla's apparatus. A motivation for such piecemeal writing is to minimize impact on regular operations (Chen, pars. 0007 & 0077).

Additionally, Chawla does not expressly teach identifying a memory type of the nonvolatile memory to determine appropriate commands to be sent. Huang teaches a processor identifying the type of flash ROM disposed on a motherboard (col. 2, lines 38-50). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply an identifying step such as Huang's to Chawla's apparatus. A motivation for doing so would have been to accommodate different types of flash ROM that require different command sets (Huang, col. 1, line 48- col. 2, line 3).

As per claim 2, Chen teaches comparing the version number of the update code and the version number of the nonvolatile memory for a given region, and executing the update program only if the version number of the update code is greater than the nonvolatile memory code version number (par. 0073).

As per claim 3, Chawla 's vital code inherently stores the version number. Chen teaches a metadata segment within an image to store the version number (pars. 0059 & 0063) and teaches retrieving the version number from the nonvolatile memory (par. 0073).

As per claim 4, Chawla teaches writing the update code, which inherently includes the version number, into that region of nonvolatile memory if the write test is successful (col. 7, lines 17-31).

As per claim 5, Chen teaches terminating the update without performing any write operations if the version number of the update code is less than or equal to the nonvolatile memory version number for each vital region (par. 0073).

As per claim 6, Chawla teaches querying a user whether the nonvolatile version number should be downgraded (col. 7, lines 41-52).

As per claim 7, Chen teaches disparate regions of nonvolatile memory (pars. 0034 & 0077).

As per claim 8, Chen teaches disparate regions of nonvolatile memory (pars. 0034 & 0077).

As per claim 9, Chen teaches disparate regions of nonvolatile memory (pars. 0034 & 0077).

As per claim 10, Chawla teaches the test code is equivalent to the update code (par. 7, lines 26-31).

As per claim 11, Chawla teaches a host bus adapter (HBA) for implementing upper layer protocols (ULPs) (col. 5, lines 56-65).

As per claim 12, Chawla teaches an Internet Small Computer System Interface (iSCSI) or a fibre channel controller circuit (col. 5, lines 56-65).

As per claim 13, Chawla teaches a host computer comprising the HBA (col. 5, lines 35-55).

As per claim 14, Chawla teaches a storage area network (SAN), wherein an iSCSI or a fibre channel network is coupled to the iSCSI or fibre channel controller circuit and one or more storage devices are coupled to the iSCSI or fibre channel network (col. 5, lines 35-55).

As per claims 15-28, since Chawla/Chen teaches the apparatus of claims 1-14, Chawla/Chen teaches the claimed computer program.

As per claims 29-38, since Chawla/Chen teaches the apparatus of claims 1-14, Chawla/Chen teaches the claimed computer method.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Albert Wang whose telephone number is 571-272-3669. The examiner can normally be reached on M-F (9:30 - 6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AW

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SUPERVISORY PATENT EXAMINER
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